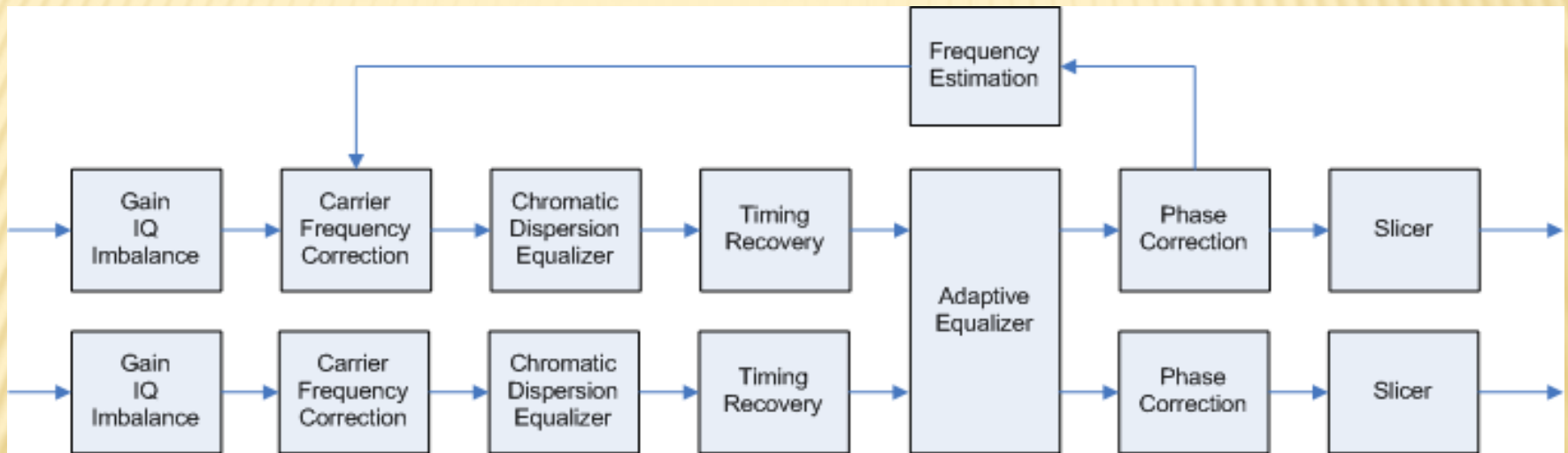


SIMPLIFIDE COHERENT OPTICAL RECEIVER ARCHITECTURE

SUMMARY

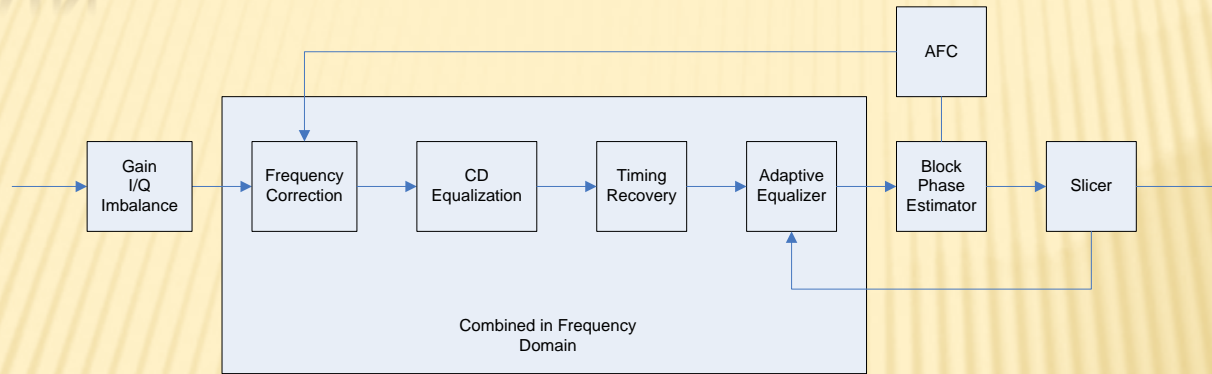
- ✘ Novel Patented Pending Architecture which Can Reduce Area of Coherent Optical Receiver by 50% or More for Depending on Implementation

SINGLE CARRIER RECEIVER ARCHITECTURE



- Basic Single Carrier MIMO Modem Architecture
- Same General Architecture for Modems for Last 20+ Years
- Optical Exception is Requirement for Chromatic Dispersion Filtering
- Architectural Issues
 - Chromatic Dispersion Filter is Extremely Large for Some Channels
 - Timing Recovery has Poor Performance related to Impairments

MOVE MOST OPERATIONS TO FREQUENCY DOMAIN

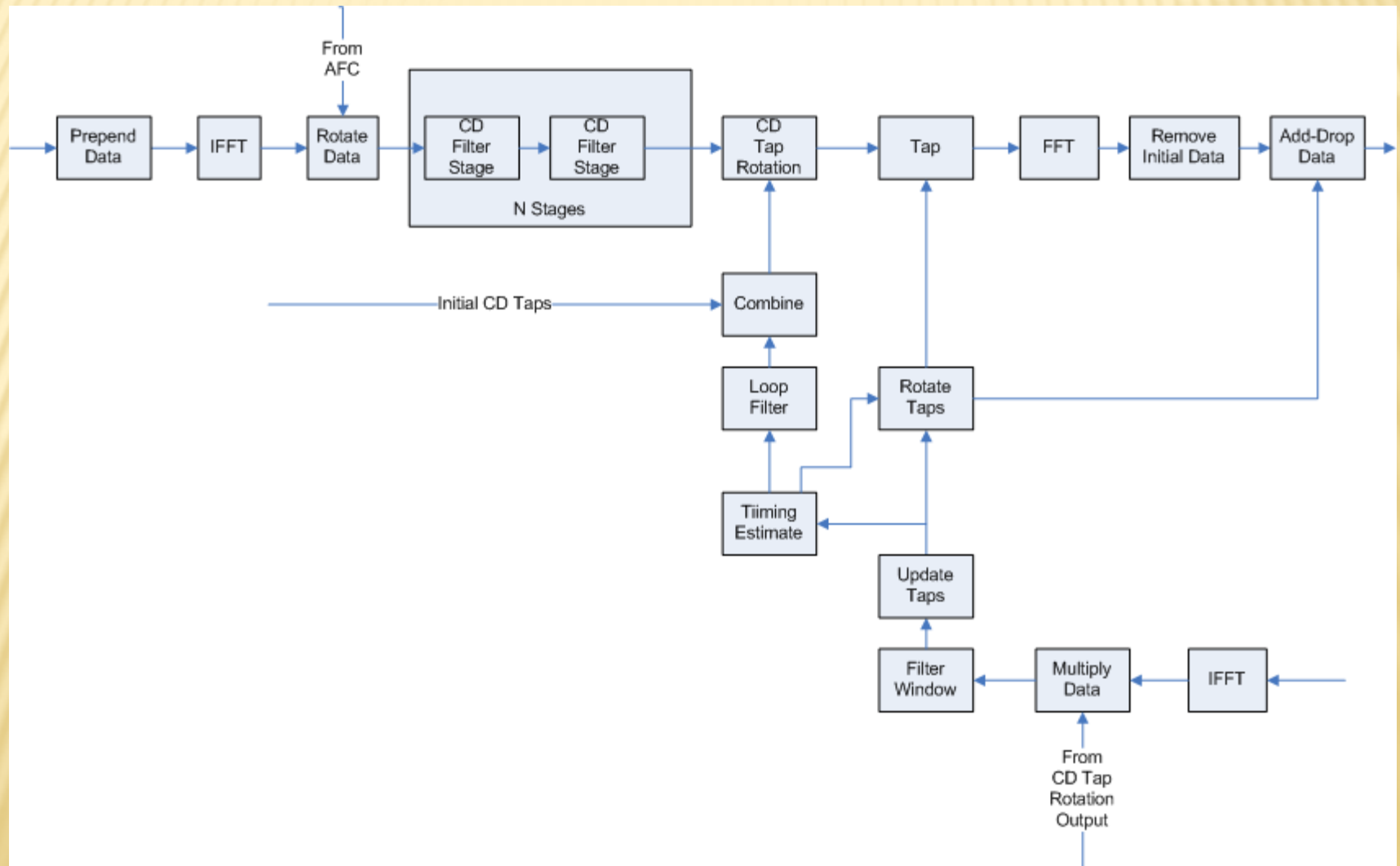


- ✘ CD and Jones Equalizers are already in frequency domain
- ✘ Issues
 - ✘ Timing Recovery is Generally Done in Time Domain
 - ✘ Different FFT Sizes between CD and Adaptive

SOLUTION

- ✘ Split Chromatic Dispersion Filter into smaller filters applied serially to reduce the FFT Size
- ✘ Perform TR in the Frequency Domain
 - + Group Delay of Equalizer as Estimator
 - + Complex Rotation for Timing Interpolation
 - + Add/Drop Samples by shifting taps and dropping data

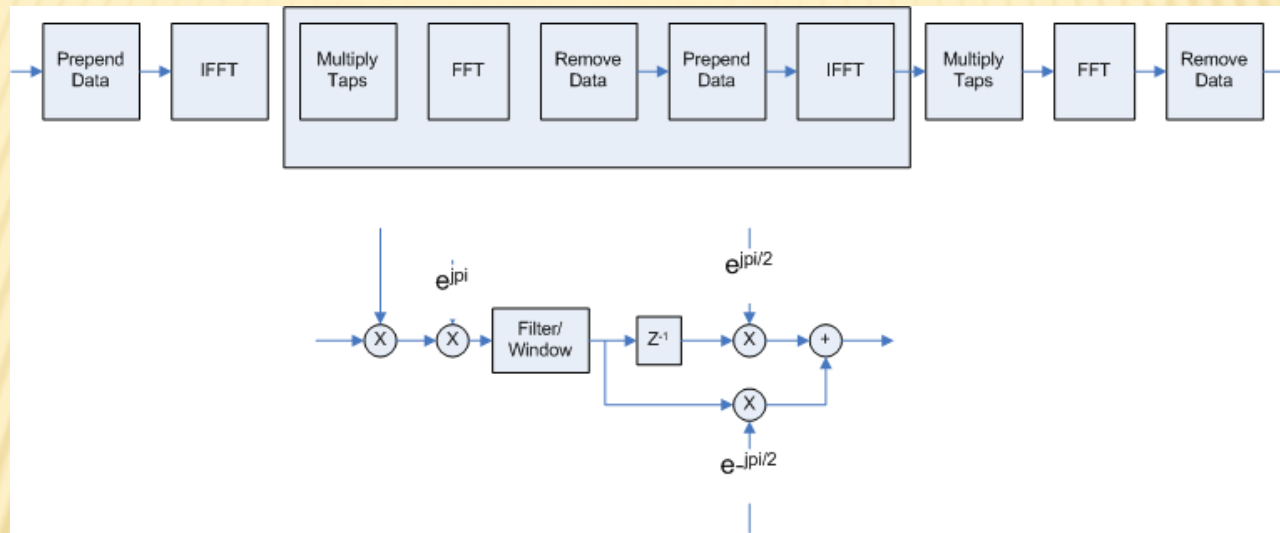
DETAILED BLOCK DIAGRAM



CHROMATIC DISPERSION FILTER

- ✘ Large Filter Converted to Concatenated Serial Filters
- ✘ Filtering Performed in Frequency Domain w/o Going Back to Time Domain
- ✘ Smaller Area than Larger Filter in Many Cases
- ✘ Requires Smaller FFT Allowing CD and Adaptive Equalizer to Be Combined
- ✘ Power Efficient as Stages can Be Bypassed when Not Required

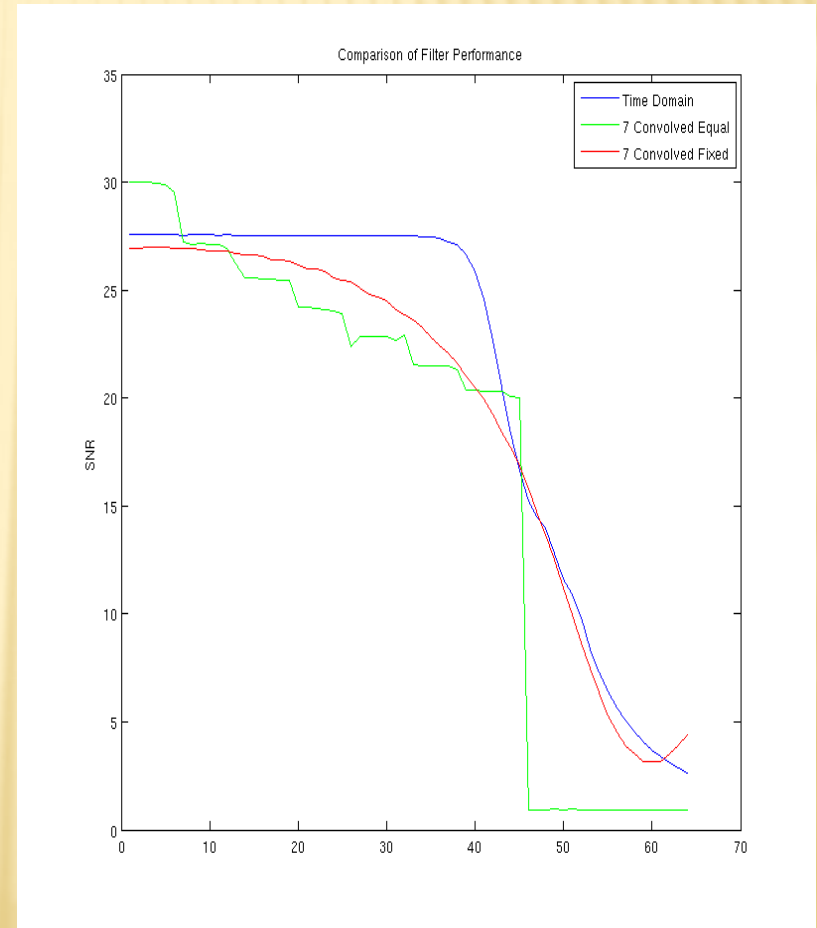
2 STAGE SERIAL FILTER EXAMPLE



- ✘ Top Diagram shows 2 Frequency Domain Filters in Series
- ✘ Bottom Diagram Shows Frequency Domain Equivalent Operation of the FFT, Data Removal, Prefix Addition and

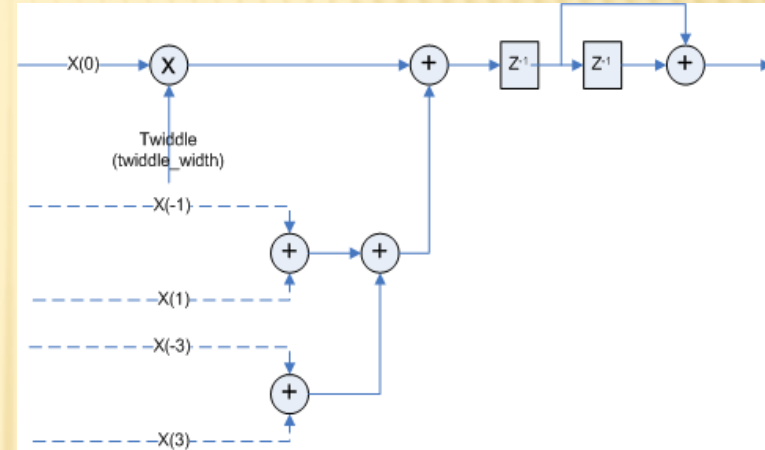
SERIAL FILTER PERFORMANCE

- ✘ 512 Tap Time Domain CD Filter versus Serial Filter
- ✘ Goal is for Serial Filters to Equal TD CD Performance
- ✘ Greater than 20dB SNR Over band of Interest which is good enough for QPSK
- ✘ Performance Easily Improved at cost of gates



CD FILTER SEGMENT AREA

		Filters	Width
CSD Multiplier		160	10
Worst Case Total Adds	20		
Worst Case Registers	6		
Remaining Logic --- Taps [1 0 -8 32 -80 1]	4		
Total Adds	10		
Total Registers	4		
Total Gates Per Input		2400	
Total Gates Per Stage		384000	
Total Gates For 7 Stages		2688000	



- ✘ The Composite Area of the Filter Stages is estimated at 2.7M Gates with a somewhat pessimistic Estimate
- ✘ Actual Gate Estimates will Be Available Soon

EFFICIENT CD STRUCTURE FOR POWER



- ✘ Power can be easily saved for smaller CD by bypassing filter stages
- ✘ Final Stage of the CD Filter can be used for timing recovery interpolation saving interpolation blocks as well

TIMING RECOVERY IN FREQUENCY DOMAIN

- ✘ Better Performance Due to Interpolation in Frequency Domain
- ✘ Timing Error Calculated by Group Delay of Frequency Domain Taps
- ✘ Tap Centering Handled Easily
- ✘ Design Complexity of Time Domain NCO Avoided

SUMMARY OF AREA REDUCTIONS

Area Additions	Area Removals
CD Filter Stages	CD FFT, CD IFFT
	Timing Recovery Interpolator, NCO
Group Delay Calculation	TR Gardner and Filtering
Circular Shift (Small Mux)	Frequency Correction Block
9 Tap Fixed Coefficient Filter	FFT and IFFT for Tap Constraint

- ✘ The Additions are dwarfed in comparison to the removals especially the CD FFTs